IN THE CLAIMS

1. (canceled)
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18. (canceled)
19. (canceled)
20. (currently amended) A method of producing a crystalline substrate based device comprising:

providing a wafer including a semiconductor substrate and comprising a plurality of semiconductor microstructures each including at least one optoelectronic device;

providing ~~at least one~~ a wafer-level transparent packaging layer;

forming a wafer-level spacer onto said ~~at least one~~ wafer-level transparent packaging layer, ~~a wafer-level spacer,~~ said packaging layer and said spacer defining a plurality of cavities extending entirely through said spacer, the step of forming the wafer-level spacer including applying a spacer

material separate from the wafer-level transparent packaging layer to the wafer-level transparent packaging layer; then

sealing said wafer-level spacer to said ~~semiconductor substrate~~wafer~~,~~ ~~thereby fully defining a gap~~ so that the cavities in the wafer-level spacer extend between ~~ones of said plurality of microstructures and corresponding chip scale portions of said at least one~~ the wafer and the transparent packaging layer~~, without requiring removal of material from said at least one transparent packaging layer overlying said at least one optoelectronic device~~; and

subsequently dicing said semiconductor substrate, having said wafer-level spacer and said ~~at least one~~ wafer-level transparent packaging layer sealed thereunto, to form individual chip scale packaged devices each including a microstructure, a chip scale portion of said transparent packaging layer, and a cavity disposed between the microstructure and the portion of the transparent packaging layer,

wherein the process is performed without removing material of the wafer-level transparent packaging layer prior to said dicing step.

21. (canceled)

22. (currently amended) A method of producing a crystalline substrate based device according to claim 20 and wherein said sealing comprises using ~~E~~epoxy to seal said wafer-level spacer onto said ~~semiconductor substrate~~wafer.

23. (previously presented) A method of producing a crystalline substrate based device according to claim 20 and wherein said semiconductor substrate comprises silicon.

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40. (currently amended) A method of producing a crystalline substrate based device according to claim ~~39~~ 20 and wherein said sealing comprises using an adhesive separate from said wafer-level spacer to seal said wafer-level spacer onto said semiconductor substrate.

41. (previously presented) A method of producing a crystalline substrate based device according to claim 40 and wherein said adhesive comprises epoxy.

42. (currently amended) A method for producing a crystalline substrate based device according to claim ~~39~~ 20 and wherein said semiconductor substrate comprises silicon.

43. (canceled)

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64. (canceled)

65. (currently amended) A method of producing a crystalline substrate based device according to claim 20 ~~wherein~~ further comprising the step of forming ~~the individual chip scale package devices have a multiplicity of~~ electrical contacts ~~plated~~ prior to completion of the dicing step so that the contacts extend away from the wafer scale transparent packaging layer and so that after completion of the dicing step the contacts extend along edge surfaces of the individual chip scale packaged devices. ~~thereof~~.

66. (canceled)

67. (canceled)

68. (new) A method according to claim 65 wherein said dicing step includes forming channels extending through said crystalline substrate.

69. (new) A method according to claim 68 further comprising the steps of depositing a layer material in said channels, said step of forming contacts being performed so that said contacts extend on said layer material.

70. (new) A method according to claim 69 further comprising the step of forming notches in said layer material within said channels so that surfaces of said layer material in said notches will constitute edge surfaces of the individual

chip scale packaged devices upon completion of the dicing step, the step of forming the contacts including forming the contacts on surfaces of the layer material in the notches.

71. (new) A method according to claim 70 further comprising the step of bonding an underlying packaging layer to a rear surface of the crystalline substrate facing away from said transparent packaging layer.

72. (new) A method according to claim 69 wherein said layer material is an epoxy.

73. (new) A method of producing a crystalline substrate based device according to claim 20 wherein said step of forming the wafer level spacer includes applying a layer of the spacer material and selectively exposing the layer of spacer material to illumination so as to form the spacer from the layer of spacer material in a pattern defined by the selective illumination .

74. (new) A method according to claim 73 wherein said spacer material is an epoxy photoresist.

75. (new) A method according to claim 20 wherein said step of forming said wafer-level spacer includes forming the wafer-level spacer as an array of separate spacer elements on said wafer-level transparent packaging element.

76. (new) A method according to claim 75 wherein said array of spacer elements includes pairs of spacer elements extending next to one another but separated from one another to define openings between them, wherein the sealing step is performed so as to position the spacer elements of each pair on mutually-adjacent ones of the microstructures in the wafer, and wherein the dicing step is performed so that the transparent wafer-level packaging element is cut in alignment with the openings.

77. (new) A method according to claim 76 wherein the sealing step includes applying an adhesive so that the adhesive

extends into the openings, and wherein the dicing step includes dicing the adhesive in the openings.

78. (new) A method according to claim 20 wherein each said optoelectronic device includes an array of microlenses, and wherein the sealing step is performed so that each array of microlenses is disposed within one of the cavities in the wafer-level spacer.

79. (new) A method of making a plurality of chip scale packages comprising:

(a) uniting a unitary semiconductor wafer including a plurality of chips, a wafer level protective layer and a plurality of spacer elements so that the spacer elements are disposed between the wafer level protective layer and the wafer, so that each spacer element is disposed on one chip and defines a cavity between that chip and the wafer level protective layer, and so that there are openings between spacer elements disposed on adjacent chips, the uniting step including connecting the spacer elements to the wafer using an adhesive so that the adhesive extends into the openings; and then

(b) dicing the wafer and wafer level protective layer along severance planes aligned with the openings and extending through the adhesive.

80. (new) A method as claimed in claim 79 wherein said uniting step includes providing the spacer elements and the wafer level protective layer as a unit and assembling the unit with the wafer.

81. (new) A method as claimed in claim 79 wherein the spacer elements are rectangular.

82. (new) A method of making a chip scale package comprising:

(a) forming a wafer level spacer on a wafer level protective layer by applying a layer of a spacer material onto the wafer level protective layer, selectively exposing the layer

of spacer material to illumination so as to form the spacer from the layer of spacer material in a pattern defined by the selective illumination; and then

(b) assembling the wafer level protective layer and wafer level spacer with a semiconductor wafer including a plurality of chips and bonding the wafer level spacer to the semiconductor wafer; and then

(c) dicing the wafer and wafer level protective layer

83. (new) A method according to claim 82 wherein said spacer material is an epoxy photoresist.

84. (new) A method according to claim 82 wherein the step of bonding the wafer level spacer to the wafer includes providing an adhesive separate from the wafer level spacer between the wafer level spacer and the semiconductor wafer.

85. (new) A method of producing a crystalline substrate based device comprising:

providing a wafer including a semiconductor substrate and comprising a plurality of semiconductor microstructures each including at least one optoelectronic image sensor;

providing a wafer-level transparent packaging layer;

forming a wafer-level spacer onto said wafer-level transparent packaging layer, said packaging layer and said spacer defining a plurality of cavities extending entirely through said spacer, the step of forming the wafer-level spacer including applying a spacer material separate from the wafer-level transparent packaging layer to the wafer-level transparent packaging layer; then

sealing said wafer-level spacer to said wafer so that the cavities in the wafer-level spacer extend between the wafer and the transparent packaging layer; and

subsequently dicing said semiconductor substrate, having said wafer-level spacer and said wafer-level transparent packaging layer sealed thereunto, to form individual chip scale

packaged devices each including a microstructure, a chip scale portion of said transparent packaging layer, and a cavity disposed between the microstructure and the portion of the transparent packaging layer,

wherein the process is performed without removing material from portions of the wafer-level transparent packaging layer overlying the image sensor prior to said dicing step.

86. (new) A method of producing a crystalline substrate based device according to claim 85 and wherein said sealing comprises using epoxy to seal said wafer-level spacer onto said wafer.

87. (new) A method of producing a crystalline substrate based device according to claim 85 and wherein said semiconductor substrate comprises silicon.

88. (new) A method of producing a crystalline substrate based device according to claim 85 and wherein said sealing comprises using an adhesive separate from said wafer-level spacer to seal said wafer-level spacer onto said semiconductor substrate.

89. (new) A method of producing a crystalline substrate based device according to claim 88 and wherein said adhesive comprises epoxy.

90. (new) A method for producing a crystalline substrate based device according to claim 85 and wherein said semiconductor substrate comprises silicon.

91. (new) A method of producing a crystalline substrate based device according to claim 85 further comprising the step of forming electrical contacts prior to completion of the dicing step so that the contacts extend away from the wafer scale transparent packaging layer and so that after completion of the dicing step the contacts extend along edge surfaces of the individual chip scale packaged devices.

92. (new) A method according to claim 91 wherein said dicing step includes forming channels extending through said crystalline substrate.

93. (new) A method according to claim 92 further comprising the steps of depositing a layer material in said channels, said step of forming contacts being performed so that said contacts extend on said layer material.

94. (new) A method according to claim 93 further comprising the step of forming notches in said layer material within said channels so that surfaces of said layer material in said notches will constitute edge surfaces of the individual chip scale packaged devices upon completion of the dicing step, the step of forming the contacts including forming the contacts on surfaces of the layer material in the notches.

95. (new) A method according to claim 94 further comprising the step of bonding an underlying packaging layer to a rear surface of the crystalline substrate facing away from said transparent packaging layer.

96. (new) A method according to claim 93 wherein said layer material is an epoxy.

97. (new) A method of producing a crystalline substrate based device according to claim 85 wherein said step of forming the wafer level spacer includes applying a layer of the spacer material and selectively exposing the layer of spacer material to illumination so as to form the spacer from the layer of spacer material in a pattern defined by the selective illumination .

98. (new) A method according to claim 97 wherein said spacer material is an epoxy photoresist.

99. (new) A method according to claim 85 wherein said step of forming said wafer-level spacer includes forming the wafer-level spacer as an array of separate spacer elements on said wafer-level transparent packaging element.

100. (new) A method according to claim 99 wherein said array of spacer elements includes pairs of spacer elements extending next to one another but separated from one another to define openings between them, wherein the sealing step is performed so as to position the spacer elements of each pair on mutually-adjacent ones of the microstructures in the wafer, and wherein the dicing step is performed so that the transparent wafer-level packaging element is cut in alignment with the openings.

101. (new) A method according to claim 100 wherein the sealing step includes applying an adhesive so that the adhesive extends into the openings, and wherein the dicing step includes dicing the adhesive in the openings.

102. (new) A method according to claim 85 wherein each said optoelectronic image sensor includes an array of microlenses, and wherein the sealing step is performed so that each array of microlenses is disposed within one of the cavities in the wafer-level spacer.